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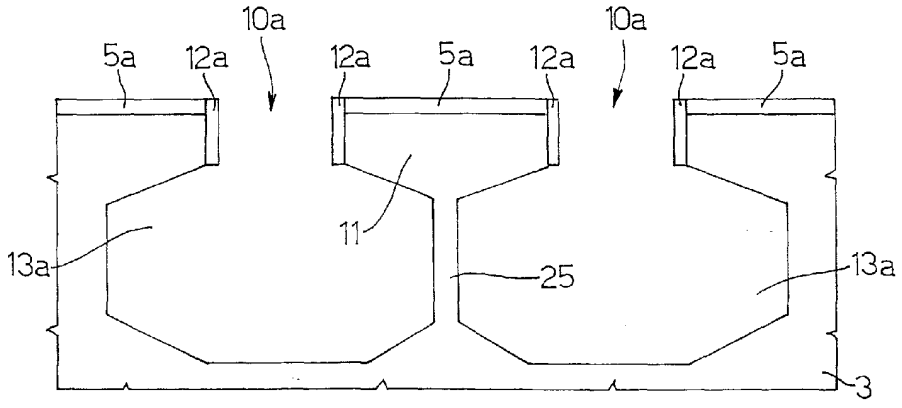
(54) Process for manufacturing a semiconductor material wafer comprising single-crystal regions separated by insulating material regions, in particular for manufacturing intergrated power devices, and wafer thus obtained

(57) The process comprises the steps of: carrying out a directional etching, in a semiconductor material body (2, 3), to form trenches (10, 10a) having a first width; carrying out an isotropic etching of the semiconductor material body (2, 3) under the trenches (10, lOa) to form cavities (13; 13a; 13b) having a width larger than the trenches; covering the walls of the cavities with dielectric material (17a; 17b; 17c); depositing non-conducting material different from thermal oxide to fill said cavities at least partially, so as to form a single-crystal island (16) separated from the rest of the semiconductor material body (2, 3). The isotropic etching permits the formation of at least two adjacent cavities (13a, 13b) separated by a support region (25) of semiconductor material which is oxidized (26) together with the walls of the cavities to provide a support to the island (16) prior to filling with non-conducting material.



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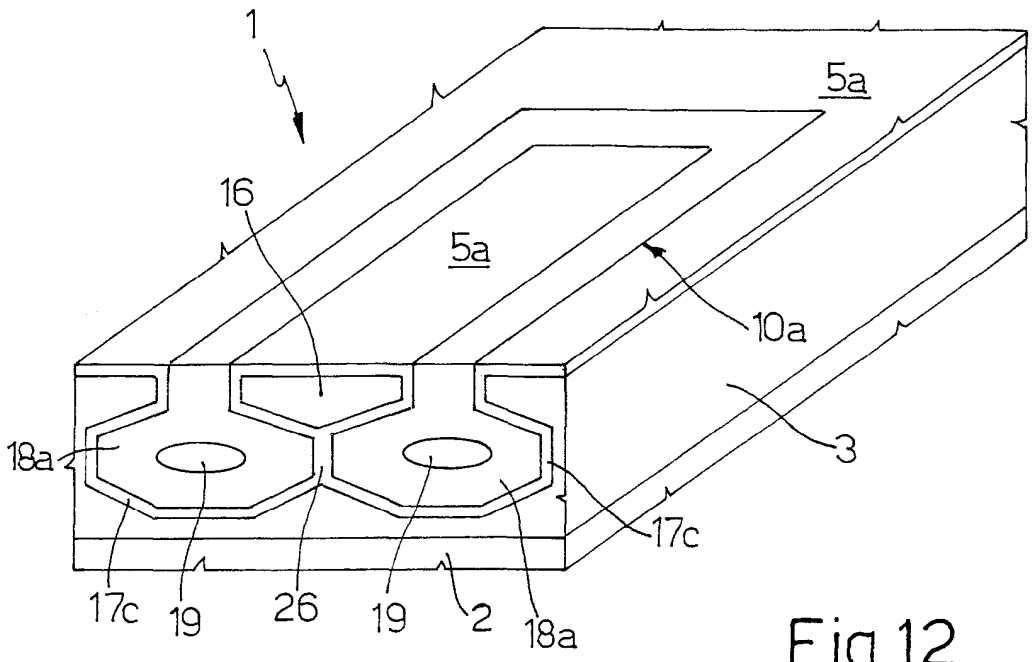

Fig.12

Description

[0001] The present invention relates to a process for manufacturing a semiconductor material wafer comprising single-crystal regions separated by insulating material regions, in particular for manufacturing integrated power devices, and wafer thus obtained.

[0002] As known, the integration of power devices with components of the control circuitry involves several problems mainly due to parasitic effects depending on undesired interactions between the power devices and the circuitry components. Conventionally, electrical isolation between various components produced on the same chip is obtained through reverse-biased PN junctions. Thereby parasitic components (such as diodes, transistors or capacitors) degrading the performance of the circuit also form besides the design components.

[0003] Parasitic elements are disadvantageously present in any type of integrated circuit, but are more problematic in power devices, above all of the vertical current flow type. In fact, the problems caused by the parasitic components depends on the values of the operating currents and voltages and, in particular, the switching speed. Furthermore, with respect to lateral devices, the vertical current flow devices have a more complex structure, composed of many active layers, and it is therefore difficult to provide a physical/mathematical model taking parasitic effects into account.

[0004] Various solutions have been proposed to solve the above problem, some of which use insulating structures of the SOI (Silicon On Insulator) type.

[0005] Manufacturing SOI structures using the technique of wafer bonding or silicon direct bonding (SDB) is described, for example, in "Silicon-on-Insulator Wafer Bonding-Wafer Thinning Technological Evaluations", by J Hausman, G A Spierings, U K P Bierman and J A Pals, Japanese Journal of Applied Physics, Vol. 28, No. 8, August 1989, pp. 1426-1443 and in "Dielectric Isolation Technologies and Power Integrated Circuits", Y Sugawara, in Smart Power ICs - Technologies and Applications, by B Murari, F Bertotti, G A Vignola, Springer, 1995, pp. 150-157. Specifically, according to this technique, the surface of two silicon wafers is oxidized, and the two wafers are bonded together, to obtain a single wafer comprising a buried oxide layer. A surface of the thus obtained wafer is then ground to reduce the thickness thereof to a desired value (typically from a few tenths to a few tens of microns) and obtain a silicon layer for accommodating the circuit components. The silicon layer and, subsequently, the oxide layer are then selectively etched where power devices are to be formed. Epitaxial growth is then carried out, to obtain islands of buried oxide separated from each other by silicon continuity regions. Finally, the active areas (the regions over the buried oxide islands), are insulated by trenches filled with dielectric material and used for the forming low-voltage circuitry while power devices with vertical current flow are formed in the continuity regions of the silicon.

[0006] In a variant of the illustrated solution, the oxide islands are formed on one of the wafers prior to bonding.

[0007] The illustrated solutions are disadvantageous because of their complexity and the cost associated in particular with some phases, such as wafer bonding to form an SOI substrate. Furthermore, the variant above described has the drawback that bonding of wafers whose surfaces are not uniform (because of the presence of silicon regions and oxide regions) is a difficult process and has low yield.

[0008] To overcome these disadvantages, European patent application No. 98830007.5 of 13.1.98 filed in the applicant's name describes a method using only conventional steps in microelectronics. Specifically, according to this method, initially a silicon wafer is recessed to form trenches having a first depth; the silicon portions adjacent to the trenches are protected with a hard mask shaped like an upturned U and the trenches are etched to a second depth. Columns or walls whose top end is protected by the hard mask form in this way. The wafer is then oxidized and the portions of the columns or walls not protected by the hard mask form silicon oxide regions expanding towards the inside the trenches, closing them. In contrast, the top end of the columns or walls is not oxidized. Therefore, at the end of the oxidation a continuous silicon oxide layer, surmounted by single-crystal silicon regions, is obtained. Finally, using the silicon of the single-crystal silicon regions as nucleus, an epitaxial growth is carried out, forming a layer which can be used for integrating electronic components.

[0009] According to a different solution, described in European patent application No. 98830299.8 of 15.5.98 in the same applicant's name, wells, of N^+ type for example, are formed in a substrate, of P type for example, by ion implantation; an epitaxial layer is then grown. Trenches extending as far as the buried wells, laterally thereto, are formed in the epitaxial layer; the buried wells are anodized, then oxidized and then removed, to create a buried air gap having above epitaxial regions of single-crystal silicon connected to each other and to the rest of the wafer by means of silicon columns. Thermal oxidation is then carried out, to grow an oxide region from the walls of the buried air gap and from the trenches, to fill the buried air gap and the trenches. At the end the epitaxial regions are completely surrounded by silicon oxide, both at the sides and at the bottom.

[0010] Finally, in European patent application No. 98830476.2 of 3.8.98 in the same applicant's name, the trenches are formed by two etching steps, firstly anisotropic and then isotropic, to widen the trenches, to reduce the thickness of the portions of the substrate to be oxidized to form the buried oxide region, before carrying out the epitaxial growth.

[0011] A drawback of the last three described solutions is that the oxide regions growing by virtue of thermal oxidation exert a pressure on the surrounding single-crystal silicon regions because of the different thermal expansion coefficients. Crystallographic defects

may therefore form in the silicon; it is not possible to eliminate these subsequently and they compromise the quality of the end product.

[0012] The object of the present invention is to provide a process for manufacturing an SOI substrate not affected by the described drawbacks and, in particular, of modest manufacture cost and high quality.

[0013] The present invention thus provides a method for manufacturing a wafer comprising first and second single-crystal regions insulated by insulating regions and a wafer thus obtained, as defined in Claim 1 and Claim 18 respectively.

[0014] For better understanding of the present invention some embodiments will now be described, purely by way of non-exhaustive example and with reference to the accompanying drawings, wherein:

- Figure 1 is a perspective view of a portion of a semiconductor material wafer in an initial manufacture step, according to a first embodiment of the present process;
- Figures 2-7 show cross-sections of the portion of wafer of Figure 1, in subsequent manufacture steps;
- Figure 8 is a perspective view of the wafer of Figure 7;
- Figure 9 shows a semiconductor material wafer similar to that of Figure 8, formed according to a second embodiment of the present process;
- Figures 10 and 11 show cross-sections similar to those of Figures 2-7, in subsequent manufacture steps according to a third embodiment of the invention;
- Figure 12 is a perspective view of the wafer of Figure 11, in a subsequent manufacture step;
- Figures 13-16 show cross-sections similar to those of Figures 2-7, in subsequent manufacture steps according to a fourth embodiment of the invention; and
- Figure 17 shows a cross-section of an integrated power circuit provided with an insulating structure formed according to the present process.

[0015] Figure 1 shows a wafer 1 of single-crystal silicon comprising a substrate 2, of N^+-type for example, doped with antimony or arsenic, and an epitaxial layer 3, of N-type for example, doped with phosphorus. The epitaxial layer 3 may optionally be formed with a double epitaxial layer, with different thicknesses and concentrations or, in general, as a multiple layer. Thickness, concentration and number of layers are dictated by the voltage value required for the end device, according to rules familiar to designers of discrete power devices.

[0016] Thick oxide regions, formed, for example, through the known technique LOCOS, are present in the epitaxial layer 3. In particular, Figure 1 shows a region of thick oxide 4; a similar region, not shown, may be provided in the portion of wafer 1 that is not shown, in symmetrical manner.

[0017] According to Figure 2, a surface 1a of wafer 1 is subjected to an oxidation process, to form a masking oxide layer 5 of a thickness of 0.5 μm for example. A trench mask 7 is then formed, covering the entire masking oxide layer 5 apart from windows 8 where trenches are to be formed. In the described embodiment, the windows 8 extend parallel to each other in a perpendicular direction to the page, between the thick oxide regions 4 (not shown).

[0018] Then, Figure 3, the exposed portions of the masking oxide layer 5 are selectively removed by oxide etching, forming masking oxide regions 5'; trench mask 7 is then removed; then epitaxial layer 3 is anisotropically etched (silicon trench etching) to obtain trenches 10 of predetermined depth, separated from each other by intermediate silicon regions 11 surmounted by oxide portions 5'. Preferably the trench etching is a dry etching, carried out in plasma.

[0019] A protective layer is then deposited, of oxide or oxide and nitride for example (with a thickness comprised between 200 and 600 Å respectively, 700 and 1500 Å), and the protective layer is directionally etched without mask, Figure 4. Given the etching anisotropy, the horizontal portions of the protective layer on the bottom of the trenches 10 and on top of the oxide portions 5' are removed, obtaining in practice protective regions 12 on the walls of the trenches 10.

[0020] Then, Figure 5, silicon is isotropically etched in plasma, for example, in the same machine used for trench etching, modifying the conditions, or in acid solution, to form cavities 13 under the trenches 10. During this step, the silicon underneath the intermediate portions 11 is completely removed and the cavities 13, joining, form a single buried air gap 15. The intermediate portions 11 now extend longitudinally, suspended between pairs of thick oxide 4 regions (one of which is visible in Figure 1) which act as support, over the buried air gap 15.

[0021] Then, Figure 6, the wafer 1 is thermally oxidized to grow an interface layer 17a, 17b of silicon oxide, covering the walls of the buried air gap 15 and of the trenches 10 respectively. The thickness of the interface layer 17a, 17b is small (equal to 200 Å for example) to prevent thermal and mechanical stresses caused by oxidation from causing crystallographic defects in the silicon of the epitaxial layer 3 or of the intermediate portions 11. Alternatively, the walls of the buried air gap 15 and of the trenches 10 may also be coated with one or more layers of dielectric material, such as deposited oxide, nitride etc.

[0022] The buried air gap 15 and the trenches 10 are then filled with insulating or poorly conducting material that may be deposited in conform or not conform way, Figure 7. Preferably, undoped multi-crystal or amorphous silicon is deposited. In this way an insulating structure 18 is formed which, together with the interface layer 17a, 17b, surrounds and insulates the intermedi-

ate portions 11 (called islands 16 below) from the epitaxial layer 3. In this step the buried air gap 15 may be totally or partially filled. In Figure 7, for example, gas pockets 19, containing gas at low pressure (such as silane or another gas present in the machine for depositing the material filling the buried air gap 15 and the trenches 10) are present inside the insulating structure 18. The gas pockets 19 do not prejudice the insulation but rather reduce the coupling capacity between the islands 16 and the epitaxial layer 3, since air is a dielectric material.

[0023] The wafer 1 is then planarized by a mechanical process or an etching for example, obtaining the structure shown in cross-section in Figure 7 and in perspective view in Figure 8; conventional processing steps are then carried out to form low-voltage electronic components inside the island 16, which thus constitutes an active area, and vertical-current-flow electronic power components inside the epitaxial layer 3 and/or the substrate 2.

[0024] According to a different embodiment, shown in Figure 9, the thick oxide regions 4 are formed with trench insulation regions, one of which is visible in Figure 9 and is shown at 4a, instead of by local oxidation. Specifically, the trench insulation regions 4a are formed first, after growing the epitaxial layer 3, excavating the epitaxial layer 3 through suitably masked anisotropic etching; coating the walls of the trenches with a thin oxide layer 20; then filling the trenches with multi-crystal or amorphous silicon 21 and then planarizing the structure. The structure of Figure 9 is then obtained, by carrying out the steps previously described with reference to Figures 2-7.

[0025] The purpose of the trench insulation regions 4a is to support the intermediate regions 11 after isotropic etching for forming the trenches 10. With respect to the embodiment of Figures 1-8, forming trench insulation regions 4a has the advantage of forming deeper islands 16. In fact, the maximum thickness of the thick oxide regions 4 formed through the LOCOS technology is 2 μm and so the regions of thick oxide 4 penetrate into the epitaxial layer 3 by 1 μm at the most, which thus also represents the maximum thickness of the islands 16. This limit does not exist, however, if trench insulation regions 4a are formed; consequently, the islands 16, which must be slightly less thick than the trench insulation regions 4a, may be formed with the desired thickness, as required by the operating voltages provided for the components to be integrated.

[0026] Figures 10-12 show a third embodiment wherein the support for the intermediate portions 11 is provided from below by the epitaxial layer 3 or the substrate 2, not removed completely during anisotropic etching. Specifically, according to the third embodiment, the initial steps described with reference to Figures 1-4 up to forming protective regions 12a are initially carried out, except the thick oxide layer 4 or 4a is not grown. Furthermore, the form of the trenches, here shown at 10a, is different from that of Figures 1-9; in particular, the trenches 10a are connected in couples, at respective ends, to form trenches of closed form, rectangular for example (see Figure 12 in particular, showing a trench 10a after filling with the insulating structure).

[0027] According to the third embodiment, Figure 10, after the protective regions 12a have been formed, silicon is isotropically etched, similararly to Figure 5; in this case, however, etching ceases before all the silicon under the intermediate portions 11 is removed, so that the cavities 13a formed on the two long sides of each trench 10a do not join but are separated by a thin wall or column 25 (Figure 10). Conveniently the thickness of the thin wall 25 is comprised between 100 and 500 nm.

[0028] Then, Figure 11, the wafer is subjected to thermal oxidation to grow the silicon oxide interface layer, shown here at 17c and covering the walls of the cavities 13a and the trenches 10a, as shown in Figure 11. During this step the thin wall 25 is completely oxidized, forming an oxide column 26; consequently, the intermediate portion 11 is electrically insulated from the epitaxial layer 3, forming the island 16. Also here, the interface layer 17c is of reduced thickness (equal to at least 50 nm for example).

[0029] Finally, the cavities 13a and the trenches 10a are filled with multi-crystal or amorphous silicon, as already described with reference to Figure 7, to form insulating structures 18a, optionally having gas pockets or bubbles 19 (Figure 12).

[0030] Figures 13-16 show a fourth embodiment of the process according to which a damage implant is first carried out, starting from a substrate 2a of N-type. To this end, a first mask 45 is formed, covering the entire surface of the substrate 2a apart from openings 46 (Figure 13). An implant of an ion, a dopant for example (such as boron, phosphorus, antimony or arsenic), shown diagrammatically by arrows 47, is then carried out so as to create damaged regions 48.

[0031] The first mask 45 is then removed; the substrate 2a is optionally subjected to a thermal implanted ion diffusion or activation step and an epitaxial layer 3a is grown, as shown in Figure 14.

[0032] Silicon trench etching is then carried out, as already described with reference to Figures 2 and 3. In particular, masking oxide regions 5a are formed and trench etching is carried out, to form trenches 10a, having a depth such as to reach the damaged regions 48. The structure of Figure 14 is obtained in this way.

[0033] After the protective regions 12a have been formed, silicon is isotropically etched, in acid environment for example, Figure 15. In certain conditions the doping material renders etching more selective, allowing a more rapid removal of the silicon from the damaged regions 48 than elsewhere; consequently, during this step asymmetrical cavities 13b are formed, mutually separated by thin walls or columns 25.

[0034] Steps similar to those described with reference to Figure 11 are then carried out. In particular, thermal

oxidation is carried out; thus the interface oxide layer 17c is formed and the thin wall 25 is completely transformed into silicon oxide (region 26). The cavities 13b and the trenches 10a are then filled with multi-crystal or amorphous silicon, forming the insulating structure 18a of Figure 16, which electrically separates the island 16 from the rest of the epitaxial layer 3a and the substrate 2a.

[0035] In this way it is possible to shape the cavities 13b in different ways and, consequently, modify the shape of the insulating structure 18a and the active area defined by the island 16 as desired. In particular, if desired, it is possible to give the island 16 a flatter shape and prevent the buried air gap 15 from widening too much towards the outside with respect to the useful zone. Furthermore it is possible to control the thickness of the thin wall 26 in a more effective manner than with a simple isotropic etching of the silicon.

[0036] According to a different embodiment of the process just described with reference to Figures 13-16, inert substances (such as silicon, argon or nitrogen) may be used instead of dopants to form the damaged regions 48. The crystallographic damage caused by the ion implant accelerates the etching speed. In this case it is not necessary to interpose thermal processes between the implant of the damaged regions 48 and the growth of the epitaxial layer 3a.

[0037] Alternatively, hydrogen or helium at high dose is implanted; micro-cavities are formed in the damaged region 48 in this way. In fact, during implantation, gas forms gaseous bubbles in the silicon, and, in a subsequent thermal process, the bubbles join, increasing in size and reducing in number. The subsequent epitaxial growth to form the epitaxial layer 3a may be carried out without damaging the micro-cavities; in this way silicon isotropic etching takes place more quickly where the micro-cavities are present, forming cavities of suitable shape at the damaged regions 48.

[0038] Finally it is also possible to proceed as described above, implanting hydrogen or helium and carrying out epitaxial growth and trench etching. An oxidation step is then carried out, thereby an oxide layer grows both on the walls of the trenches and in the damaged regions 48 where the micro-cavities are present. At the end, the damaged regions 48 are formed by silicon oxide. Oxide is then etched with hydrofluoric acid. In this way a horizontal trench is formed, the trench may be deepened by isotropically etching silicon or filled immediately with multi-crystal or amorphous silicon.

[0039] The process described has the following advantages. Primarily it is simple, of low manufacture cost and high yield, since the used individual steps are per se known and common in microelectronics and it is not necessary to bond two silicon wafers. Furthermore, forming insulating structures according to the described process requires at the most only thermal growth of thin oxide layers to cover the walls of the trenches and the buried air gap and formation of the interface layer 17 between the single-crystal silicon of the epitaxial layer 3 or the substrate 2 and the multi-crystal or amorphous silicon of the insulating structure 18; consequently, the probability is reduced of thermal and mechanical stresses associated with the oxidation process forming crystallographic defects in the silicon and large regions with a different coefficient of expansion subjecting the structure to stress during operation.

[0040] Forming support regions for the island 16 through end oxide regions 4, 4a or, preferably, columns 25, 26 permits the suspension of the island 16 (or intermediate portion 11) in a very simple and effective manner, without requiring specific manufacture steps and with high reliability and reproducibility.

[0041] Furthermore, the present process reduces the silicon area required for integrating power devices and high-speed low-voltage devices (such as components of the control circuitry of the power devices), which may be formed inside the island 16 and thus inside the power devices.

[0042] An example of integration of a power device and a low-voltage high-speed device is shown, for example, in Figure 17, relating to a bipolar power transistor 50, with vertical current flow and interdigited structure, and a PMOS transistor 51. In particular, Figure 17 shows a first half of a finger 52 of the bipolar power transistor 50, a second half of the finger 52 being symmetrical. In detail, the bipolar power transistor 50 comprises a substrate 2, of N^+-type, forming the collector of the device; an epitaxial layer 3; a buried base region 57, of P-type, and a buried emitter region 58, of N^+-type, formed above the buried base region 57 and adjacent thereto. Furthermore, Figure 17 shows a base diffusion contact region 59, of P-type; a base contact metal region 59a; an emitter diffusion contact region 60; an emitter contact metal region 60a; and a sinker region 61. The emitter diffusion contact region 60 and the sinker region 61 are both N^+-type and are formed at the same time.

[0043] An insulating structure 18a and an island 16, formed according to one of the embodiments of the present process, are present in a portion 65 of the epitaxial layer 3 included between the emitter diffusion contact region 60 and the sinker region 61, above the buried emitter region 58. Inside the island 16, defining an active area, is the PMOS transistor 51 of known structure and not therefore described in detail. Consequently, since the PMOS transistor 51 of the circuitry is disposed over the buried emitter region 58, the overall area of silicon is equal to the area occupied by the bipolar power transistor 50 alone.

[0044] The embodiment of Figure 17 also has the advantage that the PMOS transistor 51 (or another component) formed in the island 16 is dielectrically insulated from the remaining wafer since there can be no current flow between the island 16 and the rest of the epitaxial layer 3 or the substrate 2; furthermore, it is also capacitively isolated from the substrate, in that currents induced by sudden voltage fluctuations on the substrate

may not reach the components of the island 16 since they are connected to ground by the low-resistivity path constituted by the emitter (region 58). Finally, even electromagnetic interference does not reach the component integrated in the island 16 in that it is surrounded by a kind of Faraday cage, formed by the emitter (regions 58, 60, 61).

[0045] Finally, it will be evident that modifications and variants may be introduced to the described process and the wafer without departing from the scope of the present invention, as defined in the accompanying Claims. In particular, to improve the properties of the insulating structure, the interface layer may be formed by several dielectric layers; for example, besides an oxide layer (grown thermally or deposited), a silicon nitride layer may be provided.

[0046] Furthermore, the cavities may be filled with different materials. In particular, instead of multi-crystal or amorphous silicon, another insulating or poorly conducting material may be used (such as deposited oxide, TEOS - tetraethylorthosilicate or polyamide) which may be deposited in conform or not conform manner, without subjecting the silicon wafer to thermal stress.

[0047] The single-crystal region may comprise the substrate alone or several epitaxial layers grown successively with different thicknesses and conductivities, as indicated. Furthermore, the wafer thus obtained may be used for a multiplicity of applications, such as to form integrated microsensors.

[0048] Finally, the control circuit of the power transistor may be formed in a different region of the wafer while the active area formed by the island may be used for circuitry having different functions.

Claims

1. A process for manufacturing a wafer (1) of semiconductor material, characterized in that it comprises, in succession, the steps of:

   - carrying out a directional etching, in a semiconductor material body (2, 3), to form trenches (10, 10a) having a first width;
   - carrying out an isotropic etching of said semiconductor material body (2, 3) under said trenches to form cavities (13; 13a; 13b) having a second width larger than the first width;
   - covering said walls of said cavities with dielectric material (17a; 17b; 17c);
   - depositing non-conducting or poorly conducting material different from thermal oxide to at least partially fill said cavities, so as to form a single-crystal island (16) separated from said semiconductor material body (2, 3).

2. A process according to Claim 1, characterized in that said step of carrying out a directional etching comprises the step of carrying out a plasma etching.

3. A process according to Claim 1 or 2, characterized in that said step of carrying out an isotropic etching comprises the step of carrying out a plasma etching or an acid solution etching.

4. A process according to anyone of Claims 1-3, characterized in that said step of forming cavities (13a, 13b) comprises the step of forming at least two adjacent cavities separated by a support region (25) of semiconductor material and in that said step of covering said walls comprises the step of oxidizing said walls and said support region.

5. A process according to Claim 4, characterized in that said trenches (10a) are connected in couples and form a closed line.

6. A process according to one of Claims 1-3, characterized in that it comprises, prior to said step of carrying out a directional etching, the step of forming support regions (4; 4a) of insulating material, extending transversely and adjacent to ends of said trenches (10).

7. A process according to Claim 6, characterized in that said support regions (4) comprise thick oxide regions.

8. A process according to Claim 6, characterized in that said support structures (4a) comprise trenches filled with dielectric material.

9. A process according to one of Claims 4-8, characterized in that prior to said step of carrying out a directional etching the steps are carried out of carrying out a damage implant to form at least two damaged regions (48) in adjacent and non-adjacent position and growing an epitaxial layer (3) and in that said step of carrying out an isotropic etching comprises the step of removing said damaged regions.

10. A process according to Claim 9, characterized in that said step of carrying out a damage implant comprises the step of implanting a doping agent.

11. A process according to Claim 10, characterized in that said doping agent is selected from among boron, phosphorus, antimony and arsenic.

12. A process according to Claim 9, characterized in that said step of carrying out a damage implant comprises the step of implanting an inert material and generating crystallographic damage.

13. A process according to Claim 12, characterized in that said inert material is selected from among sili-

con, argon and nitrogen.

14. A process according to Claim 9, characterized in that said step of carrying out a damage implant comprises the step of implanting a gaseous material forming bubbles.

15. A process according to Claim 14, characterized in that said gaseous material is selected from among hydrogen and helium.

16. A process according to Claim 13 or 14, characterized in that after said step of carrying out a directional etching, the step of oxidizing said damaged regions is carried out and in that said step of carrying out an isotropic etching comprises the step of etching said semiconductor material body (2) and said damaged regions with hydrofluoric acid.

17. A process according to anyone of the preceding Claims, characterized in that said non-conducting or poorly conducting material is selected from the group comprising: undoped multi-crystal silicon, undoped amorphous silicon and deposited silicon oxide.

18. A wafer of semiconductor material, comprising a semiconductor material body (2, 3) surrounding an insulating structure (18, 18a) of non-conducting material, and an island (16) surrounded by said insulating structure; characterized in that it comprises a support structure (4; 4a; 26) for said island (16), arranged laterally to or under said island, between said island and said semiconductor material body (2, 3).

19. A wafer according to Claim 18, characterized in that said support structure is formed by at least one vertical support column (26) of silicon oxide extending between said semiconductor material body (2, 3) and said island (16) through the insulating structure (18a).

20. A wafer according to Claim 18, characterized in that said support structure comprises at least one end support region (4; 4a), of dielectric material, extending between said body of semiconductor material (2, 3) and said island (16) transversely and adjacent to said island.

21. A wafer according to Claim 20, characterized in that said end support region (4) comprises thick field oxide.

22. A wafer according to Claim 20, characterized in that said end support region is formed from a trench (4a) filled with dielectric material.

23. An integrated power device, comprising a semiconductor material body (2, 3) surrounding an insulating structure (18a) of non-conducting material, and an island (16) surrounded by said insulating structure; said semiconductor material body (2, 3) housing a vertical current flow, power transistor (50) including a buried conduction region (58) and said island (16) housing a low-voltage device (51), characterized in that said buried conduction region (58) is arranged under said island (16) and said insulating structure (18a).

24. A device according to Claim 23, characterized in that it comprises a vertical support column (26) of silicon oxide extending inside said insulating structure (18a) between a lower portion of said semiconductor material body (2, 3) and said island (16).

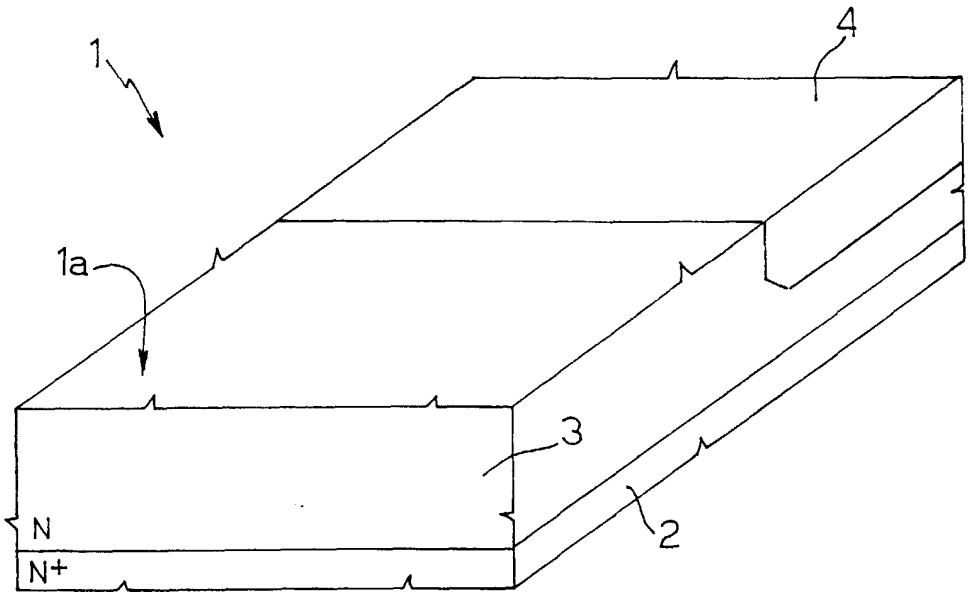

Fig. 1

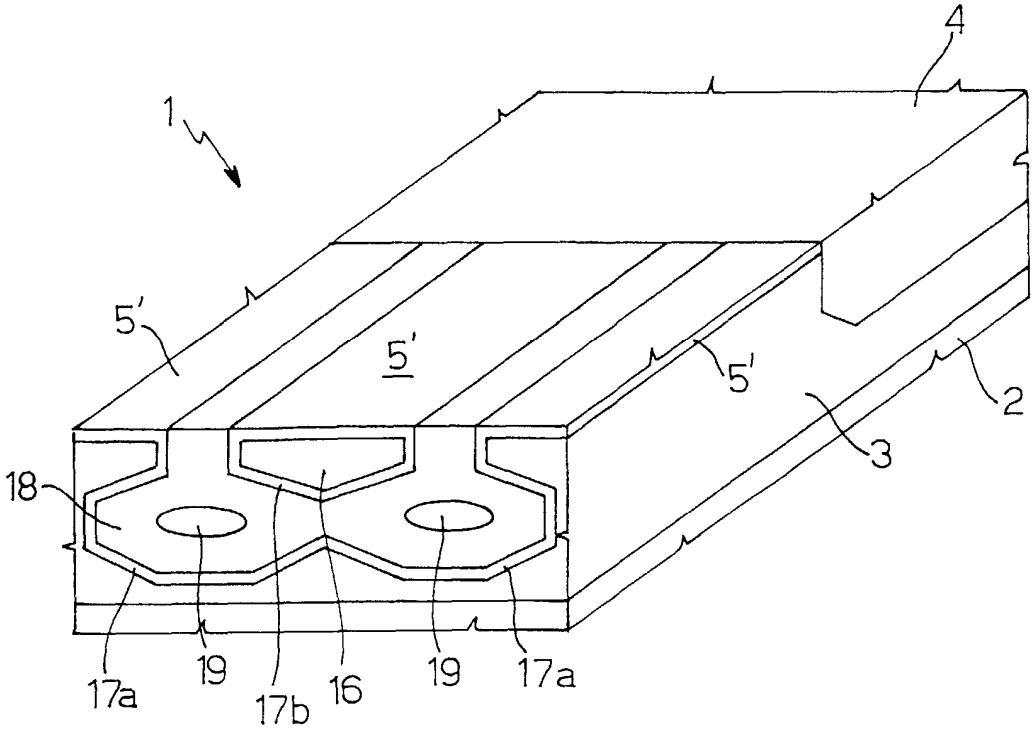

Fig. 8

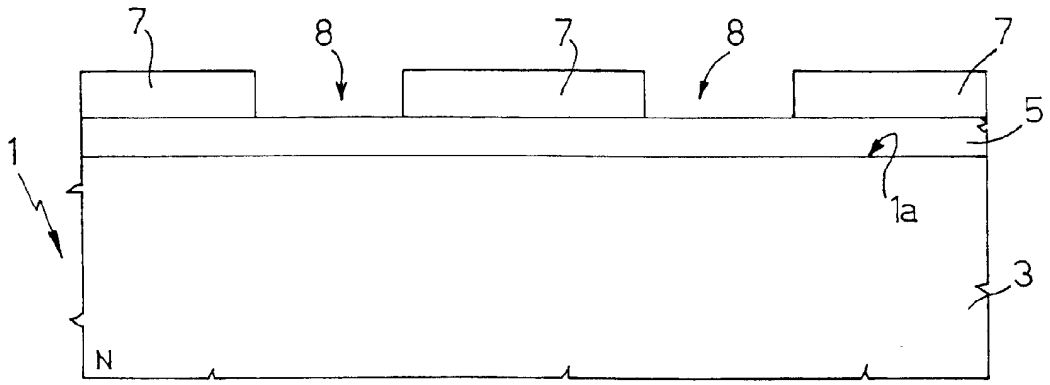

Fig. 2

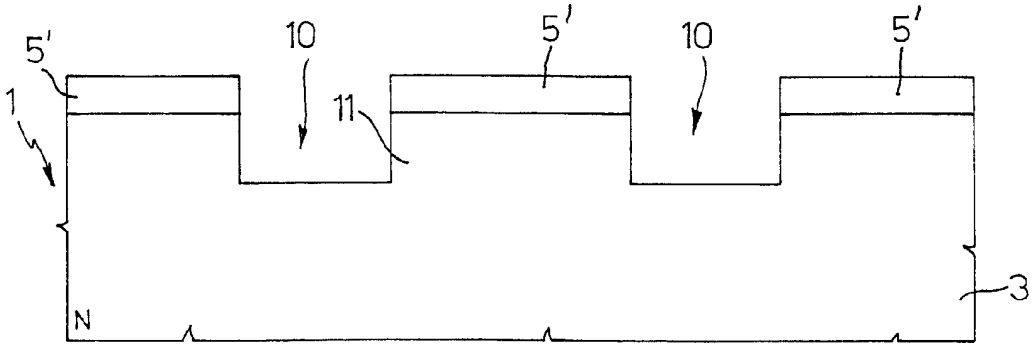

Fig. 3

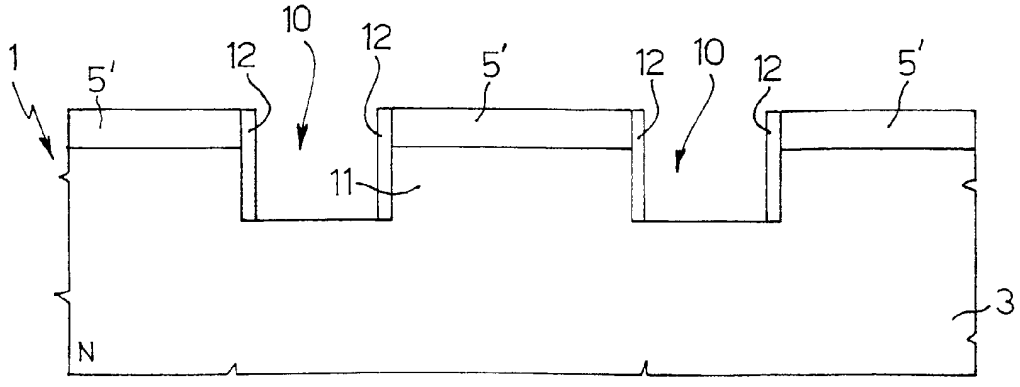

Fig. 4

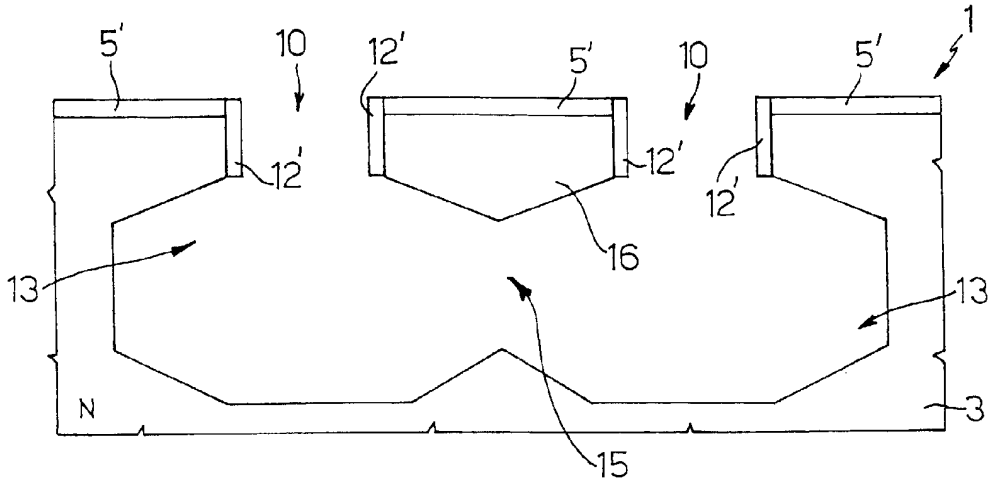

Fig. 5

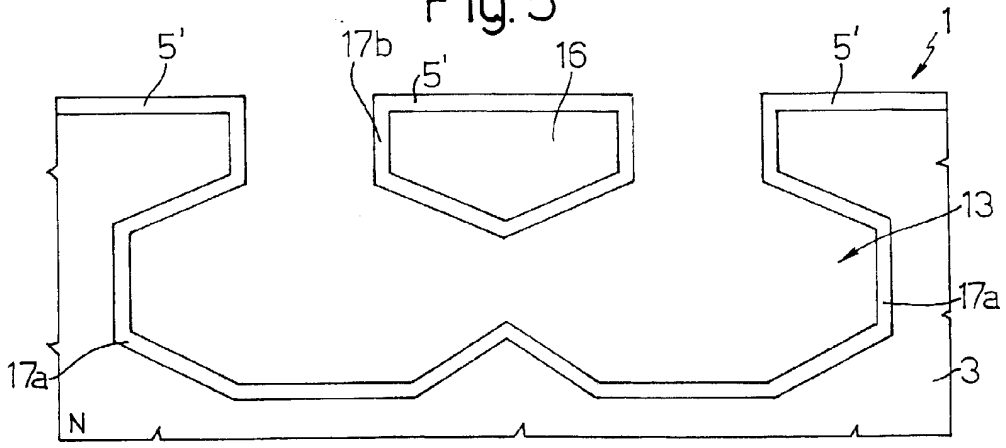

Fig. 6

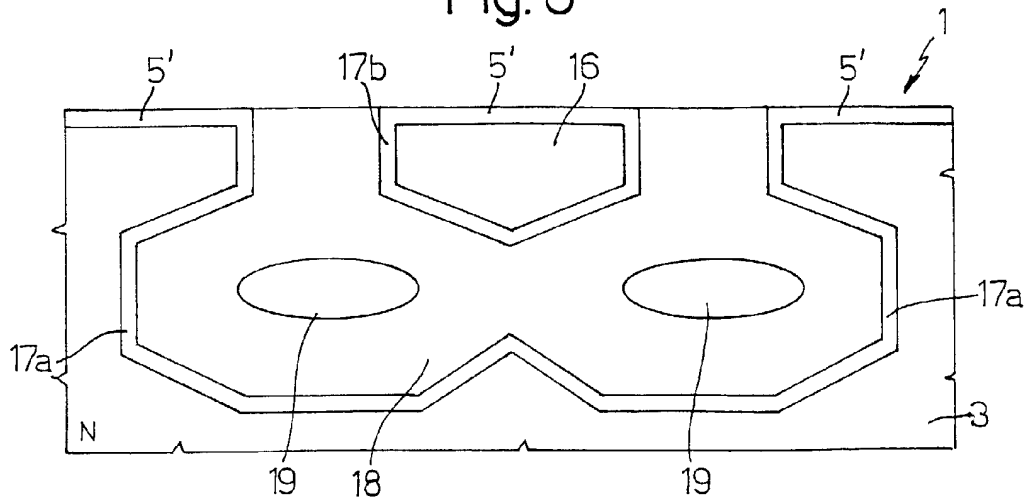

Fig. 7

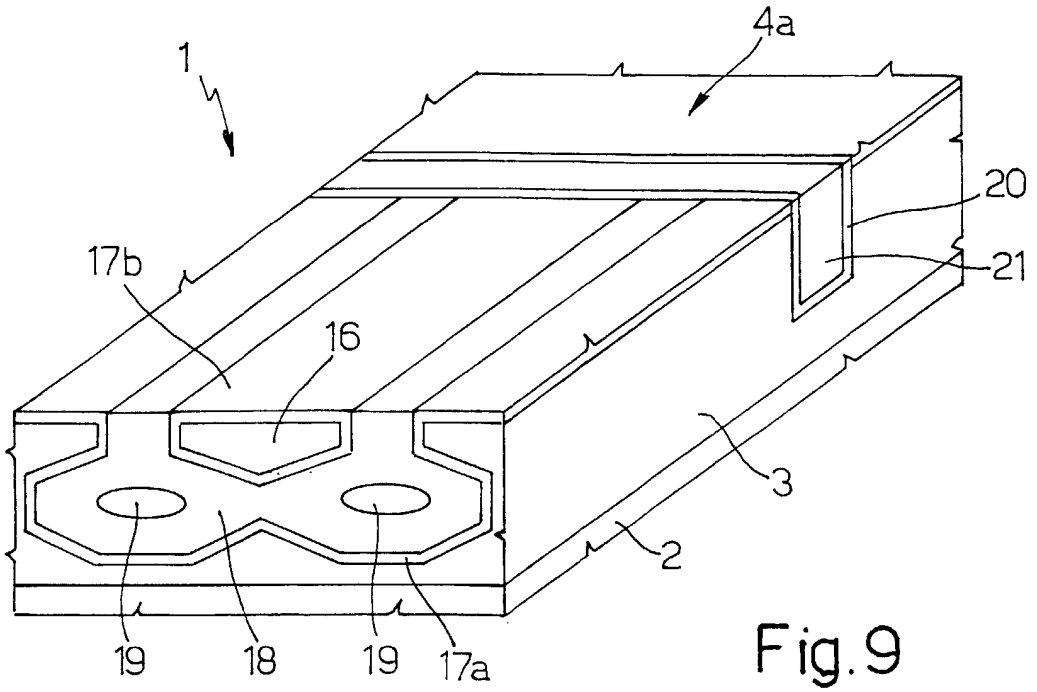
1
4a
20
21
17b
16
3
2
19
18
19
17a

Fig.9

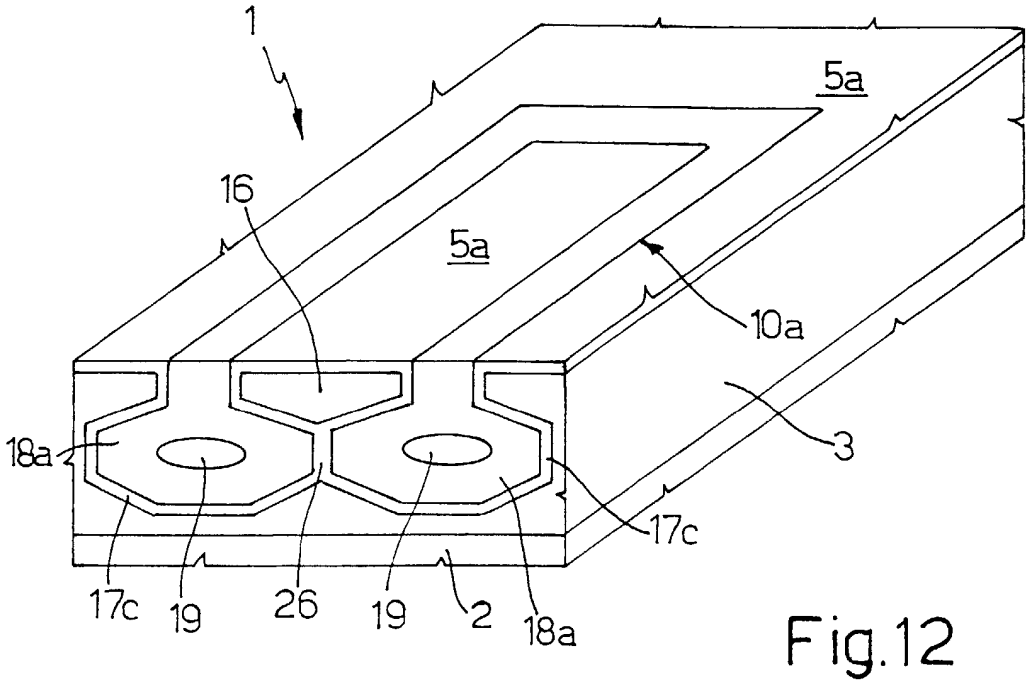
1
5a
16
5a
10a
3
18a
17c
17c
19
26
19
2
18a

Fig.12

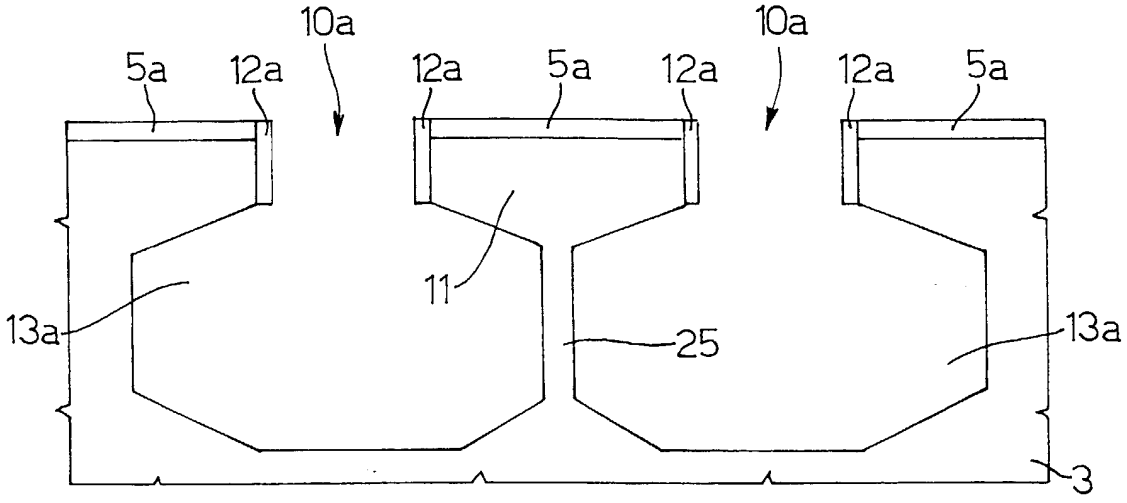
10a
10a
5a
12a
12a
5a
12a
12a
5a
11
13a
25
13a
3

Fig. 10

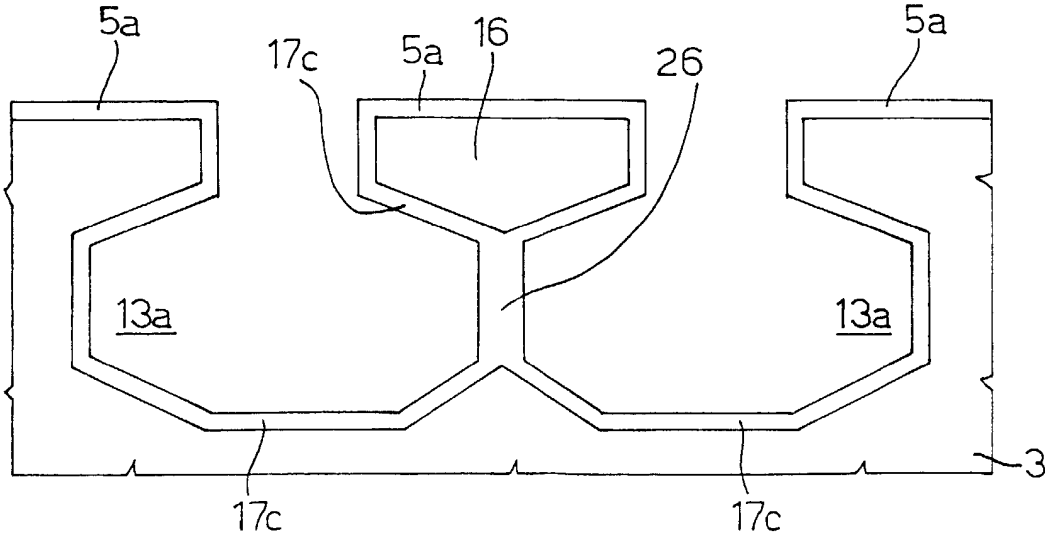
5a
17c
5a
16
26
5a
13a
13a
3
17c
17c

Fig. 11

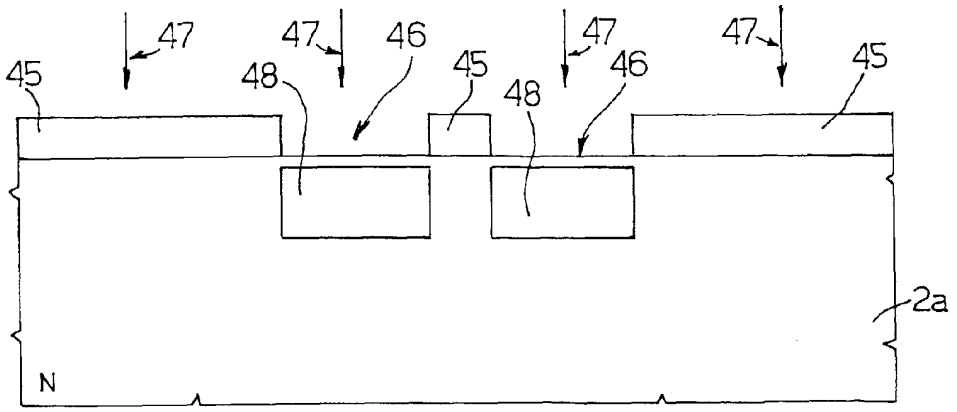

Fig. 13

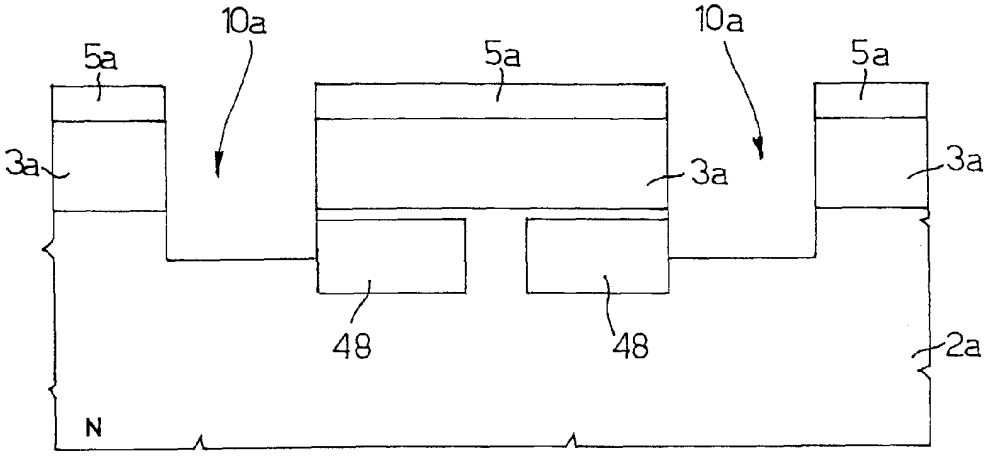

Fig. 14

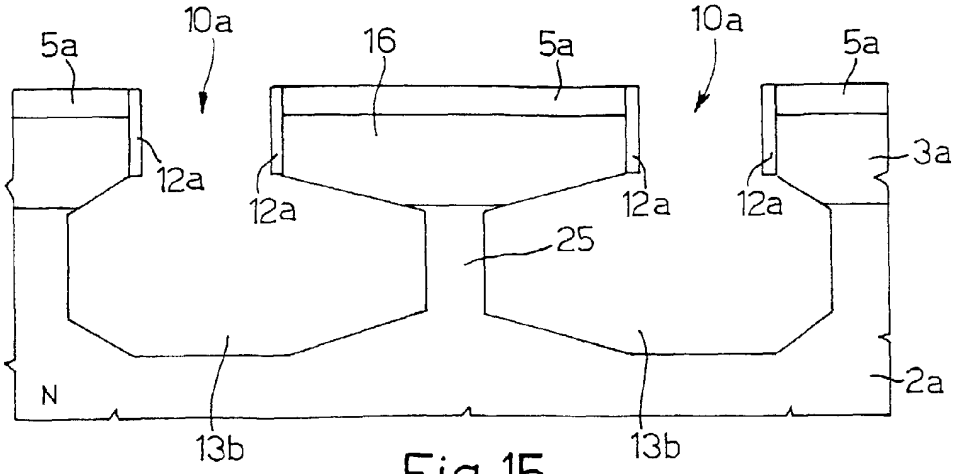

Fig. 15

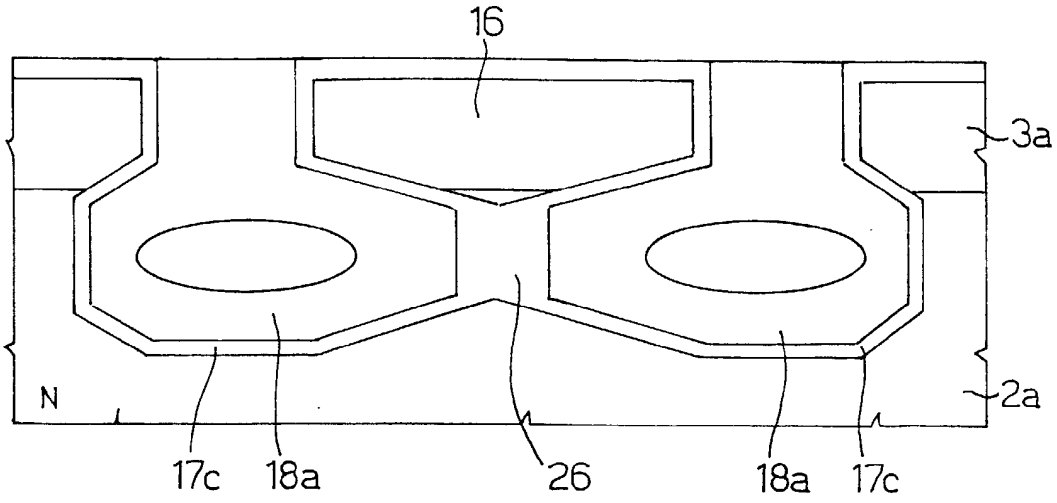
16
3a
N
2a
17c
18a
26
18a
17c

Fig.16

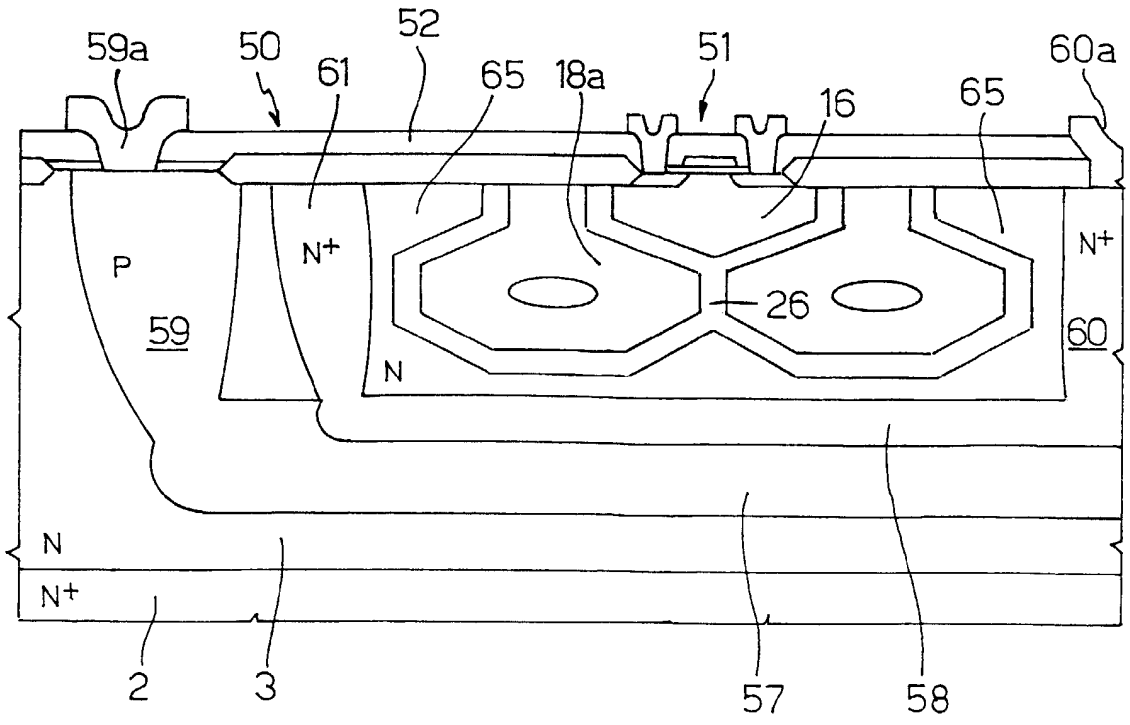
59a
50
61
52
65
18a
51
16
65
60a
P
59
N+
N
26
N+
60
N
N+
2
3
57
58

Fig.17

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0199

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 September 1999	Wirner, C

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EUROPEAN SEARCH REPORT

Application Number
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